Product Specification

80km 100GBASE-ZR4 QSFP28 Optical Transceiver Module

NS-QSFP28-100G-ZR4

PRODUCT FEATURES

- QSFP28 MSA compliant
- Compliant to 4-Wavelength WDM MSA
- Digital diagnostic monitoring support
- Hot pluggable 38 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- LC duplex connector
- Supports 103.125Gb/s aggregate bit rate
- Up to 80km transmission on single mode fiber
- Operating case temperature: 0℃ to 70℃
- Single 3.3V power supply
- RoHS-6 compliant

APPLICATIONS

- 100GBASE-ZR4 100G Ethernet
- Telecom networking

DESCRIPTIONS

QSFP28-100G-ZR4 is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.
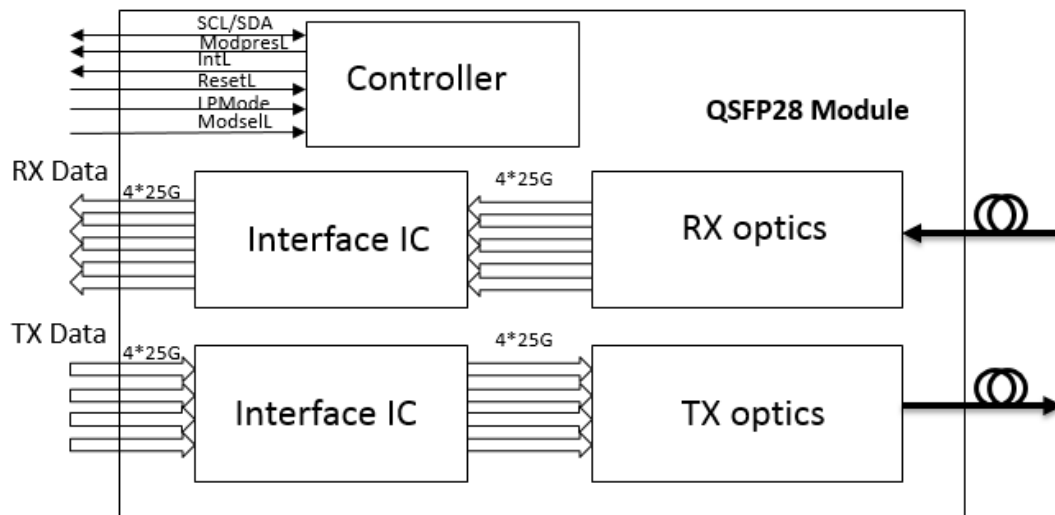
Figure 1. Transceiver Block Diagram

ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset

(t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the.

Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).
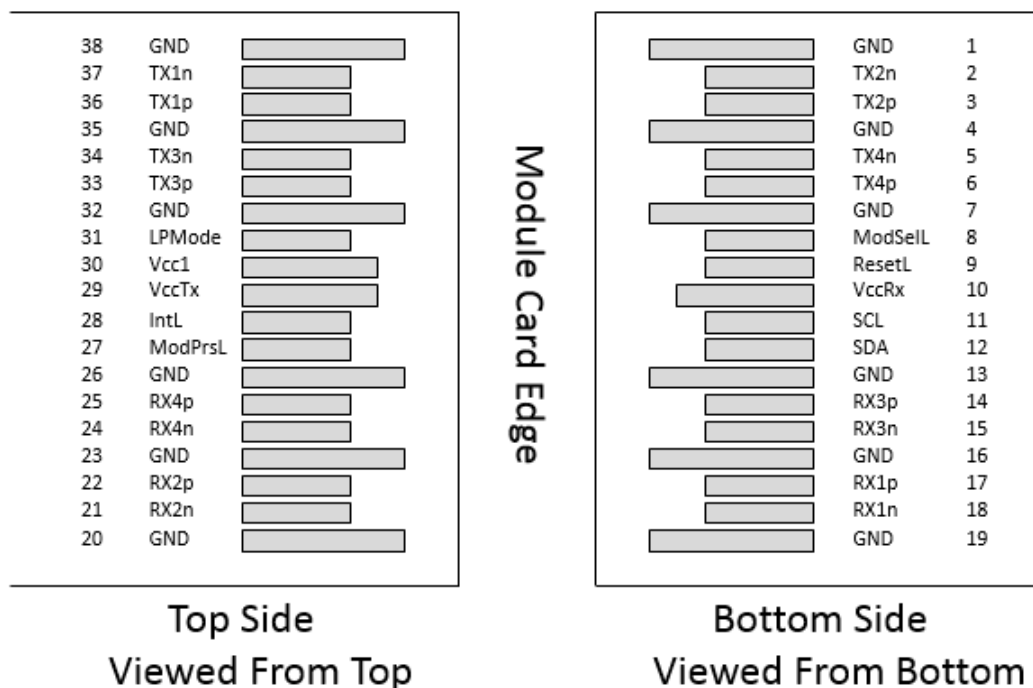
Pin Descriptions

Figure 2. MSA compliant Connector

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1

17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Non-Inverted Data Output	
25	Rx4p	Receiver Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes

1.Circuit ground is internally isolated from chassis ground.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.3	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	15		85	%	1
Damage Threshold, four lanes on	THd	5.5			dBm	

Notes

1.   Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Case Temperature	Top	0		70	℃
Link Distance with G.652				80	km

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation				6	W	
Supply Current	Icc			1.7316	A	Steady state
Transmitter						
Data Rate, each lane			25.78125		Gbps	
Differential Voltage pk-pk	Vpp			900	mV	At 1 MHz
Common Mode Voltage	Vcm	-350		2850	mV	
Transition time	Trise/Tfall	10			ps	20%~80%
Differential Termination Resistance Mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Receiver						
Data Rate, each lane			25.78125		Gbps	
Differential Termination Resistance Mismatch				10	%	At 1 MHz
		100		400		

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Differential output voltage	Vout, pp	300		600	mV	1
		400		800		
		600		1200		

Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time	Trise/Tfall	12			ps	20%~80%
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

Notes

1. Output voltage is settable in 4 discrete ranges via I2C. Default range is 400 – 800 mV.

Optical Characteristics

100GBASE-ZR4 Operation (EOL, T_{OP} = 0 to +70 C, V_{CC} = 3.135 to 3.465 Volts)

Parameters	Unit	min	type	max	Note
Transmitter					
Signaling Speed per Lane	Gb/s	25.78125 ± 100 ppm			
Transmit wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Side-Mode Suppression Ratio (SMSR)	dB	30			
Total Average Launch Power	dBm	9		12.5	
Average launch power, each lane	dBm	3		6.5	
Optical Modulation Amplitude (OMA), each lane	dBm				
Difference in launch power between any two lanes(Average and OMA)	dBm			3	
Transmitter and Dispersion Penalty (TDP), each lane	dB			TBD	
Average launch power of OFF transmitter, each lane (max)	dBm			-30	
Extinction Ratio (ER)	dB	6			

RIN OMA	dB/Hz			-130	
Optical return loss tolerance(Max)	dB			20	
Transmitter reflectance	dB			-12	

Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			1
Mask margin	%	5			
Receiver					
Signaling Speed per Lane	Gb/s	25.78125 ± 100 ppm			
Receive wavelengths	nm	1294.53		1296.59	
		1299.02		1301.09	
		1303.54		1305.63	
		1308.09		1310.19	
Average receiver power, each lane	dBm	TBD		-7	
Receiver power, each lane (OMA)	dBm				
Receiver reflectance	dB			-26	
Receiver sensitivity (OMA), each lane	dBm				
Receiver sensitivity Average, each lane	dBm			TBD	1
Stressed receiver Sensitivity (OMA), each lane	dBm				
Receiver 3 dB electrical upper cutoff frequency, each lane	GHz			31	
Damage threshold, each lane	dBm	5.5			
Saturation Power（EOL）	dBm	-7			
LOS Assert	dBm	-40			
LOS Deassert	dBm			-31	
LOS Hysteresis	dB	0.5			

Notes

1， Measured with 25.78125 Gb/s, PRBS-31 NRZ, ER>6dB (ZR4), 1260~1330nm, BER<5E-5

EEPROM Definitions

Lower Memory Map

Address	Type	Size	Name	Description	Value(Hex)	Remarks
0	R	1	Identifier	Identifier	0x11	
1	R	1	Status	Revision Compliance	0x07	

Address	Type	Size	Name	Description	Value(Hex)	Remarks
2	R	1		Flat_mem/ IntL/Data_Not_Ready		
3	R	1		Latched TX/RX LOS indicator, Channel 1~4		
4	R	1		Latched TX Adaptive EQ Fault/TX Transmitter/Laser fault indicator, Channel 1~4		
5	R	1		Latched TX CDR LOL/RX CDR LOL indicator, Channel 1~4		
6	R	1		Latched temperature high/low alarm/warning		
7	R	1		Latched supply voltage high/low alarm/warning		
8	R	1		Vendor Specific		
9	R	1		Latched RX Power High/Low Alarm/Warning, Channel 1~2		
10	R	1		Latched RX Power High/Low Alarm/Warning, Channel 3~4		
11	R	1	Interrupt Flags	Latched TX Bias High/Low Alarm/Warning, Channel 1~2		
12	R	1		Latched TX Bias High/Low Alarm/Warning, Channel 3~4		
13	R	1		Latched TX Power High/Low Alarm/Warning, Channel 1~2		
14	R	1		Latched TX Power High/Low Alarm/Warning, Channel 3~4		
15	R	1		Reserved		
16	R	1				
17	R	1				
18	R	1				
19	R	1		Vendor Specific		
20	R	1				
21	R	1				
22	R	1	Free Side	Internally measured temperature (MSB)		
23	R	1		Internally measured temperature (LSB)		
24	R	1		Reserved		
25	R	1				
26	R	1		Internally measured supply voltage (MSB)		

27	R	1	Device	Internally measured supply voltage (LSB)		
28	R	1	Monitors	Reserved		
29	R	1				
30	R	1		Vendor Specific		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
31	R	1				
32	R	1				
33	R	1				
34	R	1		Internally measured RX input power, channel 1 (MSB)		
35	R	1		Internally measured RX input power, channel 1 (LSB)		
36	R	1		Internally measured RX input power, channel 2 (MSB)		
37	R	1		Internally measured RX input power, channel 2 (LSB)		
38	R	1		Internally measured RX input power, channel 3 (MSB)		
39	R	1		Internally measured RX input power, channel 3 (LSB)		
40	R	1		Internally measured RX input power, channel 4 (MSB)		
41	R	1		Internally measured RX input power, channel 4 (LSB)		
42	R	1	Channel Monitors	Internally measured TX bias, channel 1 (MSB)		
43	R	1		Internally measured TX bias, channel 1 (LSB)		
44	R	1		Internally measured TX bias, channel 2 (MSB)		
45	R	1		Internally measured TX bias, channel 2 (LSB)		
46	R	1		Internally measured TX bias, channel 3 (MSB)		
47	R	1		Internally measured TX bias, channel 3 (LSB)		
48	R	1		Internally measured TX bias, channel 4 (MSB)		
49	R	1		Internally measured TX bias, channel 4 (LSB)		
50	R	1		Internally measured TX Power, channel 1 (MSB)		
51	R	1		Internally measured TX Power, channel 1 (LSB)		
52	R	1		Internally measured TX Power, channel 2 (MSB)		
53	R	1		Internally measured TX Power, channel 2 (LSB)		
54	R	1		Internally measured TX Power, channel 3 (MSB)		
55	R	1		Internally measured TX Power, channel 3 (LSB)		
56	R	1		Internally measured TX Power, channel 4 (MSB)		
57	R	1		Internally measured TX Power, channel 4 (LSB)		
58	R	1				
59	R	1				
60	R	1				

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61	R	1	Reserved channel monitor set 4		
62	R	1			
63	R	1			
64	R	1			

Address	Type	Size	Name	Description	Value(Hex)	Remarks
65	R	1				
66	R	1		Reserved channel monitor set 5		
67	R	1				
68	R	1				
69	R	1				
70	R	1				
71	R	1				
72	R	1				
73	R	1				
74	R	1		Vendor Specific		
75	R	1				
76	R	1				
77	R	1				
78	R	1				
79	R	1				
80	R	1				
81	R	1				
82	R	1	Reserved	Reserved		
83	R	1				
84	R	1				
85	R	1				
86	RW	1	Control	TX Disable, channel 1~4		
87	RW	1		RX_Rate_select, channel 1~4		
88	RW	1		TX_Rate_select, channel 1~4		
89	RW	1		RX4_Application_Select		
90	RW	1		RX3_Application_Select		
91	RW	1		RX2_Application_Select		
92	RW	1		RX1_Application_Select		

93	RW	1		High Power Class Enable/Power set/Power over-ride		
94	RW	1		TX4_Application_Select		
95	RW	1		TX3_Application_Select		
96	RW	1		TX2_Application_Select		
97	RW	1		TX1_Application_Select		
98	RW	1		TX/RX CDR_control, channel 1~4	0xff	
99	RW	1	Reserved	Reserved		
100	RW	1	Free Side Device and Channel Masks	Masking Bit for TX/RX LOS indicator, channel 1~4	0x00	
101	RW	1		Masking Bit for TX Adaptive EQ fault/TX Transmitter/Laser fault indicator, channel 1~4	0x00	
102	RW	1		Masking Bit for TX/RX CDR Loss of Lock indicator, channel 1~4	0x00	

Address	Type	Size	Name	Description	Value(Hex)	Remarks
103	RW	1		Masking Bit for Temperature High/Low Alarm/Warning	0x00	
104	RW	1		Masking Bit for Vcc High/Low Alarm/Warning	0x00	
105	RW	1	Vendor Specific	Vendor Specific		
106	RW	1				
107	RW	1	Reserved	Reserved		
108	R	1	Free Side Device Properties	Propagation Delay MSB		
109	R	1		Propagation Delay LSB		
110	R	1		Advanced Low Power Mode/Far Side Managed/Min Operating Voltage		
111	RW	1	Assigned for use by PCI Express	Assigned for use by PCI Express		
112	RW	1				
113	R	1	Free Side Device Properties	Far End Implementation/Near End Implementation		
114	RW	1	Reserved	Reserved		
115	RW	1				
116	RW	1				
117	RW	1				
118	RW	1				
119	W	1	Password Change Entry Area			
120	W	1				
121	W	1				
122	W	1				
123	W	1	Password Entry Area			
124	W	1				
125	W	1				
126	W	1				
127	RW	1	Page Select Byte	Page Select		

Upper Memory Map Page 00h

Address	Type	Size	Name	Description	Value(Hex)	Remarks
128	R	1	Identifier	Identifier Type of free side device	0x11	

129	R	1	Ext. Identi-fier	Extended Identifier Type of free side device		
130	R	1	Connector Type	Code for connector type	0x07	
131	R	1		10/40G/100G Ethernet Compliance Codes	0x80	

Address	Type	Size	Name	Description	Value(Hex)	Remarks
132	R	1	Specification Compliance	SONET Compliance Codes	0x00	
133	R	1		SAS/SATA Compliance Codes	0x00	
134	R	1		Gigabit Ethernet Compliance Codes	0x00	
135	R	1		Fibre Channel link length/Fibre Channel Transmitter Technology	0x00	
136	R	1		Fibre Channel Transmitter Technology	0x00	
137	R	1		Fibre Channel transmission media	0x01	
138	R	1		Fibre Channel Speed	0x00	
139	R	1	Encoding	Code for serial encoding algorithm	0x03	
140	R	1	BR, nominal	Nomial bit rate, units of 100 Mbps. For BR > 25.4G, set this to FFh and use Byte 222	0xff	
141	R	1	Extended Rate Select Compliance	Tags for extended rate select compliance		
142	R	1	Length (SMF)	Link length supported for SMF fiber in km	0x50	
143	R	1	Length (OM3 50 um)	Link length supported for EBW 50/125 um fiber (OM3), units of 2 m	0x00	
144	R	1	Length (OM2 50 um)	Link length supported for EBW 50/125 um fiber (OM2), units of 1 m	0x00	
145	R	1	Length (OM1 62.5 um)	Link length supported for 62.5/125 um fiber (OM1), units of 1 m	0x00	
146	R	1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147	0x00	
147	R	1	Device technology	Device technology	0x64	
148	R	1			0x48	

149	R	1	Vendor name	"HISILICON" in ASCII	0x49	
150	R	1			0x53	
151	R	1			0x49	
152	R	1			0x4c	
153	R	1			0x49	
154	R	1			0x43	
155	R	1			0x4f	

Address	Type	Size	Name	Description	Value(Hex)	Remarks
156	R	1			0x4e	
157	R	1			0x20	
158	R	1			0x20	
159	R	1			0x20	
160	R	1			0x20	
161	R	1			0x20	
162	R	1			0x20	
163	R	1			0x20	
164	R	1	Extended Module	Extended Module codes for InfiniBand		
165	R	1	Vendor OUI	Free side device vendor IEEE company ID		
166	R	1				
167	R	1				
168	R	1	Vendor PN	Part number provided by free side device vendor(ASCII)	0x4f	
169	R	1			0x4d	
170	R	1			0x39	
171	R	1			0x35	
172	R	1			0x35	
173	R	1			0x38	
174	R	1			0x5a	
175	R	1			0x53	
176	R	1			0x31	
177	R	1			0x30	
178	R	1			0x30	
179	R	1			0x20	
180	R	1			0x20	
181	R	1			0x20	
182	R	1			0x20	
183	R	1			0x20	
184	R	1	Vendor rev	Revision level for part number provided by vendor(ASCII)		
185	R	1				
186	R	1	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)	0x66	1310nm
187	R	1			0x58	
188	R	1	Wavelength tolerance or Copper Cable Attenuation	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tol.=value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12GHz (Byte 189)	0x01	±2nm
189	R	1			0x90	
190	R	1	Max case temp.	Maximum case temperature in degrees C	0x46	

Address	Type	Size	Name	Description	Value(Hex)	Remarks
191	R	1	CC_BASE	Check code for base ID fields (Bytes 128-190)		
192	R	1	Link codes	Extended Specification Compliance Codes	0x00	
193	R	1	Options	Rate Select, TX Disable, TX Fault, LOS, Warning indicators for: Temperature, VCC, RX power, TX Bias, TX EQ, Adaptive TX EQ, RX EMPH, CDR Bypass, CDR LOL Flag.		
194	R	1				
195	R	1				
196	R	1	Vendor SN	Serial number provided by vendor (ASCII)		
197	R	1				
198	R	1				
199	R	1				
200	R	1				
201	R	1				
202	R	1				
203	R	1				
204	R	1				
205	R	1				
206	R	1				
207	R	1				
208	R	1				
209	R	1				
210	R	1				
211	R	1				
212	R	1	Date Code	Vendor's manufacturing date code		
213	R	1				
214	R	1				
215	R	1				
216	R	1				
217	R	1				
218	R	1				
219	R	1				
220	R	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved.		
221	R	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device.		
222	R	1	BR, nominal	Nominal bit rate per channel, units of 250 Mbps. Complements Byte 140.	0x70	
223	R	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)		

224	R	1	Vendor Specific	Vendor Specific EEPROM		
225	R	1				
226	R	1				

Address	Type	Size	Name	Description	Value(Hex)	Remarks
227	R	1				
228	R	1				
229	R	1				
230	R	1				
231	R	1				
232	R	1				
233	R	1				
234	R	1				
235	R	1				
236	R	1				
237	R	1				
238	R	1				
239	R	1				
240	R	1				
241	R	1				
242	R	1				
243	R	1				
244	R	1				
245	R	1				
246	R	1				
247	R	1				
248	R	1				
249	R	1				
250	R	1				
251	R	1				
252	R	1				
253	R	1				
254	R	1				
255	R	1				

Digital Diagnostic Monitoring Functions

QSFP28-100G-ZR4 support the I2C-based Diagnostic Monitoring Interface (DMI) defined in document SFF-8636. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes(A0 memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3°C	1，2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 49	< 10%	2
Transmitter optical power	50 to 57	< 3dB	2
Receiver optical power	34 to 41	< 3dB	2

Alarm and Warning Thresholds

QSFP28-100G-ZR4 support alarms function, indicating the values of the preceding basic perfor- mance are lower or higher than the thresholds.

| Performance Item	Alarm Threshold Bytes(A0[03] memory)	Unit	Low threshold	High threshold
Temp Alarm	128 to 131	℃	-10	80
Temp Warning	132 to 135	℃	0	70
Voltage Alarm	144 to 147	V	2.97	3.63
Voltage Warning	148 to 151	V	3.135	3.465
TX Power Alarm	192 to 195	dBm	0	8.2
TX Power Warning	196 to 199	dBm	3	6.5
RX Power Alarm	176 to 179	dBm	-33	-4
RX Power Warning	180 to 183	dBm	-30	-7

Mechanical Specifications
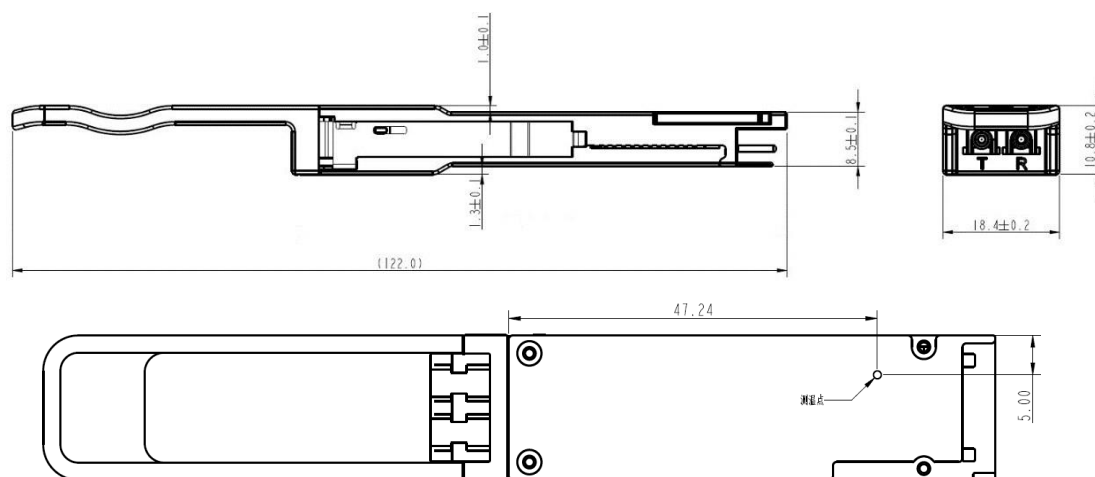
Figure 3. Mechanical Dimensions

In order to ensure the accuracy of the test, it is proposed to use the T 0.08mm type thermocouple as the standard test wire which can be pasted at the shell temperature test point with the glue(recommended Le Tai 416).

ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold value	Notes
ESD of high-speed pins	1KV	Human Body Model
ESD of low-speed pins	2KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	

Safety Specification Design

⚠ Cautions

Do not look into fiber end faces without eye protection using an optical meter (such as magnifier and microscope) within 100 mm, unless you ensure that the laser output is disabled. When operating an optical meter, observe the operation requirements.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Description
QSFP28-100G-ZR4	100GBASE-ZR4 80km QSFP28, Pull-tap, refer to Figure 3